WHAT IS CLAIMED IS:

1. A method of trimming a feature patterned on a photoresist layer, the photoresist layer disposed over a substrate and the feature including a top portion and lateral surfaces, the method comprising the steps of:

modifying the top portion of the feature patterned on the photoresist layer in an ion-dominated environment to form a modified top portion; and

trimming the feature patterned on the photoresist layer to form a trimmed feature, wherein a vertical trim rate and a lateral trim rate are associated with the feature and the vertical trim rate is slower than the lateral trim rate due to the modified top portion.

2. The method of claim 1, wherein the modifying step includes flood exposing the feature to ions.

3. The method of claim 2, wherein the modifying step includes bombarding or fluorinating the top portion with the ions for the top portion to undergo a reduction in reactivity.

4. The method of claim 2, wherein the vertical trim rate is a function of at least one of a dose of the ions and a species of the ions.

5. The method of claim 2, wherein a vertical thickness of the modified top portion is a function of at least one of an energy of the ions and a mass of the ions.

6. The method of claim 1, wherein the trimmed feature has a sub-lithographic lateral dimension.

7. The method of claim 1, wherein the trimming step includes plasma etching the feature.

8. The method of claim 1, further comprising removing the modified top portion after the trimming step.

9. An integrated circuit fabrication process, the process comprising:

developing a patterned photoresist layer, the patterned photoresist layer including at least one feature;

modifying the patterned photoresist layer to form a top portion and a bottom portion of the at least one feature, the top portion having a top etch rate and the bottom portion having a bottom etch rate, wherein the top etch rate is different from the bottom etch rate; and

trimming the patterned photoresist layer to change the at least one feature to have a sub-lithographic lateral dimension, whereby a sufficient vertical thickness exists to maintain pattern integrity, wherein the modifying step is performed after the developing step and before the ashing step.

10. The process of claim 9, wherein modifying the patterned photoresist layer includes hardening the top portion.

11. The process of claim 10, wherein modifying the patterned photoresist layer includes flood exposing the patterned photoresist layer to a beam of ions.

12. The process of claim 11, wherein trimming the patterned photoresist layer includes minimally consuming the top portion and laterally etching the bottom portion.

13. The process of claim 12, wherein a majority of the top portion and a laterally trimmed bottom portion comprises the at least one feature upon completion of the ashing step, the laterally trimmed bottom portion having the sub-lithographic lateral dimension and the sufficient vertical thickness to maintain pattern integrity.

14. The process of claim 13, further comprising removing the majority of the top portion after the ashing step to form a trimmed feature.

15. The process of claim 12, further comprising selecting parameters associated with the beam of ions to configure at least one of a thickness and the top etch rate of the top portion.

16. An integrated circuit having a feature of sub-lithographic dimension, the feature formed by the process comprising:

patterning the feature on a photoresist layer disposed over a substrate, the feature patterned in accordance with a radiation at a lithographic wavelength and a pattern provided on a mask or a reticle;

developing the feature patterned on the photoresist layer;

changing at least a portion of the photoresist layer, wherein a top portion of the feature patterned on the photoresist layer is changed to have a different etch rate from a bottom portion of the feature patterned on the photoresist layer;

trimming the feature patterned on the photoresist layer to a sub-lithographic dimension; and

transferring the trimmed feature patterned on the photoresist layer to the substrate, wherein the feature in the substrate has the sub-lithographic dimension.

17. The process of claim 16, wherein the changing step includes ion implanting the photoresist layer to form the top portion.

18. The process of claim 17, wherein the top portion has a slower etch rate relative to the bottom portion.

19. The process of claim 18, wherein the top portion has a negligible etch rate during the trimming step.

20. The process of claim 17, wherein the ion implantation comprises implanting at least one of Ar+, F+, and Kr+ ions.

21. The process of claim 20, wherein parameters associated with the ion implantation are Ar ions at an energy of approximately 1 keV and a dose of approximately 1 x 10^{13} ions/cm^2.

22. The process of claim 16, further comprising removing the top portion after the trimming step and before the transferring step.

23. The process of claim 16, wherein the lithographic wavelength of the radiation is 193 nm and the sub-lithographic dimension of the feature is approximately 150 nm.

24. The process of claim 16, wherein the sub-lithographic dimension of the feature is in the range of 30-120 nm smaller than the feature developed on the photoresist layer.